



### Description

#### PIXEL CIRCUIT, DISPLAY DEVICE, AND METHOD OF DRIVING PIXEL CIRCUIT TECHNICAL FIELD

[0001] The present invention relates to a pixel circuit having an electro-optical element controlled in luminance by a current value in an organic EL (electroluminescence) display etc., and more particularly, among image display devices in which these pixel circuits are arranged in a matrix, to a so-called active matrix type image display device in which the value of the current flowing in each electro-optical element is controlled by an insulating gate type field effect transistor provided inside each pixel circuit, and a method of driving the pixel circuit.

#### BACKGROUND ART

[0002] In an image display device, for example, a liquid crystal display etc., the image is displayed by arranging a large number of pixels in a matrix and controlling the intensity of light for each pixel in accordance with image information to be displayed.

[0003] The same is also true for an organic EL display etc., but an organic EL display is a so-called self light emission type display having a light emitting element in each pixel circuit and has the advantages that the viewability of the image is high in comparison with a liquid crystal display, no backlight is necessary, the response speed is fast, and so on.

[0004] Further, this is very different from a liquid crystal display in the point that the luminance of each light emitting element can be controlled by the value of the current flowing through it so as to obtain scales of color, that is, each light emitting element is a current controlled type.

[0005] In an organic EL display, in the same way as a liquid crystal display, the simple

matrix system and the active matrix system are possible as the method for driving the same. The former is simple in structure, but has the problems that realization of a large sized and high definition display is difficult and so on. Therefore, there has been much development work on the active matrix system for controlling the current flowing in the light emitting element inside each pixel circuit by an active element provided inside the pixel circuit, generally a TFT (thin film transistor).

[0006] FIG. 1 is a block diagram showing the configuration of a general organic EL display device.

[0007] This display device, as shown in FIG. 1, has a pixel array 2 comprised of pixel circuits (PXLC) 2a arranged in an  $m \times n$  matrix, a horizontal selector (HSEL) 3, a write scanner (WSCN) 4, data lines DTL1 to DTLn selected by the horizontal selector 3 and supplied with data signals in accordance with the luminance information, and scanning lines WSL1 to WSLm selected and driven by the write scanner 4.

[0008] Note that the horizontal selector 3 and the write scanner 4 are sometimes formed on polycrystalline silicon or formed on the periphery of the pixels by MOSIC etc.

[0009] FIG. 2 is a circuit diagram showing an example of the configuration of the pixel circuit 2a of FIG. 1 (see for example Patent Documents 1 and 2).

[0010] The pixel circuit of FIG. 2 has the simplest circuit configuration among the large number of circuits proposed and is a circuit of the so-called two-transistor drive system.

[0011] The pixel circuit 2a of FIG. 2 has a p-channel thin film field effect transistor (hereinafter referred to as an TFT) 11 and TFT 12, a capacitor C11, and a light emitting element constituted by an organic EL element (OLED) 13. Further, in FIG. 42, DTL indicates the data line, and WSL indicates the scanning line.

[0012] The organic EL element has a rectification property in many cases, so sometimes is called an OLED (organic light emitting diode). The symbol of a diode is used as the light emitting element in FIG. 2 and other figures, but a rectification property is not always required for the OLED in the following explanation.

[0013] In FIG. 2, a source of the TFT 11 is connected to a power supply potential VCC, and a cathode of the light emitting element 13 is connected to a ground potential GND. The operation of the pixel circuit 2a of FIG. 2 is as follows.

[0014] Step ST1:

[0015] When the scanning line WSL is in a selected state (low level here) and a write potential Vdata is supplied to the data line DTL, the TFT 12 becomes conductive and the capacitor C11 is charged or discharged, and a gate potential of the TFT 11 becomes Vdata.

[0016] Step ST2:

[0017] When the scanning line WSL is in a non-selected state (high level here), the data line DTL and the TFT 11 are electrically disconnected, but the gate potential of the TFT 11 is held stably by the capacitor C11.

[0018] Step ST3:

[0019] The current flowing in the TFT 11 and the light emitting element 13 becomes a value in accordance with a voltage Vgs between the gate and source of the TFT 11, and the light emitting element 13 continuously emits light with a luminance in accordance with the current value.

[0020] As in above step ST1, the operation of selecting the scanning line WSL and

transferring the luminance information given to the data line to the inside of the pixel will be called "writing" below.

[0021] As explained above, in the pixel circuit 2a of FIG. 2, when once writing the Vdata, during the period up to when next rewriting the data, the light emitting element 13 continues emitting light with a constant luminance.

[0022] As explained above, in the pixel circuit 2a, by changing the gate voltage of the drive transistor constituted by the TFT 11, the value of the current flowing in the EL light emitting element 13 is controlled.

[0023] At this time, the source of the p-channel drive transistor 11 is connected to a power supply potential VCC, so this TFT 11 is constantly operating in the saturated region. Accordingly, it becomes a constant current source having a value shown in the following equation 1.

[0024] (Equation 1)  $I_{ds} = 1/2 \cdot \mu (W/L) C_{ox} (V_{gs} - |V_{th}|)^2 \quad \dots(1)$

[0025] Here,  $\mu$  indicates the mobility of a carrier,  $C_{ox}$  indicates a gate capacitance per unit area,  $W$  indicates a gate width,  $L$  indicates a gate length,  $V_{gs}$  indicates a gate-source voltage of the TFT 11, and  $V_{th}$  indicates a threshold value of the TFT 11.

[0026] In a simple matrix type image display device, each light emitting element emits light only at an instant when it is selected, but in contrast, in an active matrix, as explained above, the light emitting element continues emitting light even after the end of writing, therefore this becomes advantageous especially in a large sized and high definition display in the point that a peak luminance and a peak current of the light emitting element can be lowered in comparison with the simple matrix.

[0027] FIG. 3 is a diagram showing aging of the 10 current-voltage (I-V) characteristic of

an organic EL element. In FIG. 3, the curve indicated by a solid line indicates the characteristic at the time of an initial state, and the curve indicated by a broken line indicates the characteristic after the aging.

[0028] In general, the I-V characteristic of the organic EL element deteriorates when time passes as shown in FIG. 3.

[0029] However, the two-transistor drive of FIG. 2 is a constant current drive, therefore a constant current continuously flows in the organic EL element as explained above. Even when the I-V characteristic of the organic EL element deteriorates, the light emission luminance thereof will not deteriorate by aging.

[0030] The pixel circuit 2a of FIG. 2 is configured by a p-channel TFT, but if it could be configured by an n-channel TFT, it would become possible to use a usual amorphous silicon (a-Si) process in TFT fabrication. By this, a reduction of the cost of the TFT substrate would become possible.

[0031] Next, a pixel circuit replacing the transistor by an n-channel TFT will be considered.

[0032] FIG. 4 is a circuit diagram showing a pixel circuit replacing the p-channel TFT of the circuit of FIG. 2 by an n-channel TFT.

[0033] A pixel circuit 2b of FIG. 4 has an n-channel TFT 21 and TFT 22, a capacitor C21, and a light emitting element constituted by an organic EL element (OLED) 23. Further, in FIG. 4, DTL indicates the data line, and WSL indicates the scanning line.

[0034] In this pixel circuit 2b, a drain side of the drive transistor constituted by the TFT 21 is connected to the power supply potential VCC, and the source is connected to an anode of the EL element 23 to thereby form a source-follower circuit.

[0035] FIG. 5 is a diagram showing operation points of the drive transistor constituted by the TFT 21 and the EL element 23 in the initial state. In FIG. 5, an abscissa indicates a drain/source voltage  $V_{ds}$  of the TFT 21, and an ordinate indicates a drain/source current  $I_{ds}$ .

[0036] As shown in FIG. 5, the source voltage is determined by the operation points of the drive transistor constituted by the TFT 21 and the EL element 23. The voltage thereof has a different value according to the gate voltage.

[0037] This TFT 21 is driven in a saturated region, therefore a current  $I_{ds}$  having a current value shown in the above equation 1 flows concerning  $V_{gs}$  with respect to the source voltage of the operation point.

[0038] Patent Document 1: U.S. Pat. No. 5,684,365

[0039] Patent Document 1: Japanese Patent Publication (A) No. 8-234683

## DISCLOSURE OF THE INVENTION

[0040] Problem to be Solved by the Invention

[0041] However, here as well, the I-V characteristic of the EL element deteriorates in the same way by aging. As shown in FIG. 6, the operation point fluctuates by this aging deterioration, therefore, even when the same gate voltage is applied, the source voltage fluctuates.

[0042] Due to this, the gate/source voltage  $V_{gs}$  of the drive transistor constituted by the TFT 21 changes, and the value of flowing current fluctuates. Simultaneously, the value of the current flowing in the EL element 23 changes, therefore, when the I-V characteristic

of the EL element 23 deteriorates, in the source-follower circuit of FIG. 4, the light emission luminance changes by aging.

[0043] Further, as shown in FIG. 7, a circuit configuration connecting the source of the drive transistor constituted by the n-channel TFT 31 to the ground potential GND, connecting the drain to the cathode of the EL element 33, and connecting the anode of the EL element 33 to the power supply potential VCC can be considered.

[0044] With this system, in the same way as a drive operation by the p-channel TFT of FIG. 2, the potential of the source is fixed. Therefore, the drive transistor constituted by the n-channel TFT 31 operates as the constant current source and can prevent a change in luminance due to the deterioration of the I-V characteristic of the EL element 33.

[0045] With this system, however, it is necessary to connect the drive transistor to the cathode side of the EL element. This cathode connection requires new development of the anode/cathode electrodes. This is considered to be very difficult by the current art.

[0046] From the above, in the usual approach, an organic EL element using an n-channel transistor not changing in luminance has not yet been developed.

[0047] Further, even developing an organic EL element using an n-channel transistor not changing in luminance, the TFT transistor is generally characterized in that the variations of mobility  $\mu$  and threshold values  $V_{th}$  are large, therefore even when a voltage having the same value is supplied to the gate of the drive transistor, the current value varies for each pixel according to the mobility  $\mu$  and threshold value  $V_{th}$  of the drive transistor, so a uniform image quality cannot be obtained.

[0048] An object of the present invention is to provide a pixel circuit in which a source-follower output free from luminance deterioration can be obtained even when the current-voltage characteristic of a light emitting element changes by aging, a source-follower

circuit of an n-channel transistor becomes possible, an n-channel transistor can be used as the drive element of the optical element by using current anode/cathode electrodes as they are, and uniform, high quality images can be displayed without regard as to variations of threshold values and mobilities of the active elements inside the pixel, a display device, and a method of driving a pixel circuit.

[0049] Means for Solving the Problem

[0050] To achieve the above object, according to a first aspect of the present invention, there is provided a pixel circuit for driving an electro-optical element changing in luminance according to a flowing current, comprising a data line to which a data signal in accordance with a luminance information is supplied; first, second, third, and fourth nodes; first and second reference potentials; a reference current supplying means for supplying a predetermined reference current; an electric connecting means connected to the second node; a pixel capacitor element connected between the first node and the second node; a coupling capacitor element connected between the electric connecting means and the fourth node; a drive transistor forming a current supply line between a first terminal and a second terminal and controlling a current flowing in the current supply line in accordance with the potential of the control terminal connected to the second node; a first switch connected between the first node and the third node; a second switch connected between the third node and the fourth node; a third switch connected between the first node and a fixed potential; a fourth switch connected between the second node and a predetermined potential line; a fifth switch connected between the data line and the fourth switch; and a sixth switch connected between the third node and the reference current supplying means, wherein, between the first reference potential and the second reference potential, the current supply line of the drive transistor, the first node, the third node, the first switch, and the electro-optical element are connected in series.

[0051] Preferably, the electric connecting means includes an interconnect for directly connecting the second node and the coupling capacitor element.

[0052] Preferably, the electric connecting means includes a seventh switch selectively connecting the second node and the coupling capacitor element.

[0053] Preferably, it includes a seventh switch connected between the first node and the electro-optical element and an eighth switch connected between the first node and the data line.

[0054] Alternatively, it includes a seventh switch connected between the first node and the electro-optical element and an eighth switch connected between the first node and the fourth node.

[0055] Preferably, the predetermined potential line is shared together with the data line.

[0056] Further, the drive transistor is a field effect transistor, a source is connected to the third node, and a drain is connected to the first reference potential.

[0057] Preferably, when the electro-optical element is driven, as a first stage, in a state where the first, second, fourth, fifth, and sixth switches are held in a non-conductive state, the third switch is held in the conductive state and the first node is connected to a fixed potential; as a second stage, the second, fourth, and sixth switches are held in the conductive state, a predetermined potential is input to the second node, the reference current flows in the third node, and the predetermined potential is charged in the pixel capacitor element; as a third stage, the second and sixth switches are held in the non-conductive state, further the fourth switch is held in the non-conductive state, the fifth switch is held in the conductive state, the data propagated through the data line is input to the second node, then the fifth switch is held in the non-conductive state; and as a fourth stage, the first switch is held in the conductive state, and the third switch is held in the non-conductive state.

[0058] Alternatively, preferably, when driving the electro-optical element, as a first stage, in a state where the first, second, fourth, fifth, sixth, and seventh switches are held in the non-conductive state, the third switch is held in the conductive state, and the first node is connected to the fixed potential; as a second stage, the second, fourth, sixth, and seventh switches are held in the conductive state, the data potential propagated through the data line is input to the second node, the reference current flows in the third node, and a predetermined potential is charged in the pixel capacitor element; as a third stage, the second and sixth switches are held in the non-conductive state, further the fourth switch is held in the non-conductive state, the fifth switch is held in the conductive state, the data propagated through the data line is input to the second node via the fourth node, then the fifth and seventh switches are held in the non-conductive state; and as a fourth stage, the first switch is held in the conductive state, and the third switch is held in the non-conductive state.

[0059] According to a second aspect of the present invention, there is provided a display device comprising a plurality of pixel circuits arranged in a matrix; data lines interconnected for each column of a matrix array of the pixel circuits and supplied with a data signal in accordance with the luminance information; first and second reference potentials; and a reference current supplying means for supplying a predetermined reference current, wherein the pixel circuit has an electro-optical element changing in luminance according to a flowing current; first, second, third, and fourth nodes; an electric connecting means connected to the second node; a pixel capacitor element connected between the first node and the second node; a coupling capacitor element connected between the electric connecting means and the fourth node; a drive transistor forming a current supply line between a first terminal and a second terminal and controlling a current flowing in the current supply line in accordance with the potential of the control terminal connected to the second node; a first switch connected between the first node and the third node; a second switch connected between the third node and the fourth node; a third switch connected between the first node and a fixed potential; a fourth switch connected between the second node and a predetermined potential line; a

fifth switch connected between the data line and the fourth switch; and a sixth switch connected between the third node and the reference current supplying means, and, between the first reference potential and the second reference potential, the current supply line of the drive transistor, the first node, the third node, the first switch, and the electro-optical element are connected in series.

[0060] According to a third aspect of the present invention, there is provided a method for driving a pixel circuit having an electro-optical element changing in luminance according to a flowing current, a data line to which a data signal in accordance with luminance information is supplied; first, second, third, and fourth nodes; first and second reference potentials; a reference current supplying means for supplying a predetermined reference current; an electric connecting means connected to the second node; a pixel capacitor element connected between the first node and the second node; a coupling capacitor element connected between the electric connecting means and the fourth node; a drive transistor forming a current supply line between a first terminal and a second terminal and controlling a current flowing in the current supply line in accordance with the potential of the control terminal connected to the second node; a first switch connected between the first node and the third node; a second switch connected between the third node and the fourth node; a third switch connected between the first node and a fixed potential; a fourth switch connected between the second node and a predetermined potential line; a fifth switch connected between the data line and the fourth switch; and a sixth switch connected between the third node and the reference current supplying means, wherein the current supply line of the drive transistor, the first node, the third node, the first switch, and the electro-optical element are connected in series between the first reference potential and the second reference potential, comprising steps of holding the third switch in the conductive state and connecting the first node to a fixed potential in the state where the first, second, fourth, fifth, and sixth switches are held in the non-conductive state; holding the second, fourth, and the sixth switches' in the conductive state and inputting the predetermined potential to the second node, sending the reference current in the third node, and charging the predetermined potential in the pixel capacitor

element; holding the second and sixth switches in the non-conductive state, and further holding the fourth switch in the non-conductive state, holding the fifth switch in the conductive state and inputting the data propagated through the data line to the second node, then holding the fifth switch in the non-conductive state; and holding the first switch in the conductive state and holding the third switch in the non-conductive state.

[0061] According to the present invention, at the time of for example the light emission state of the electro-optical element, the first switch is held in an ON state (conductive state), and the second to seventh switches are held in an OFF state (non-conductive state).

[0062] The drive transistor is designed so as to operate in the saturated region, and the current  $I_{ds}$  flowing in the electro-optical element takes a value shown by the above equation 1.

[0063] Next, the first switch becomes OFF, and the third switch becomes ON in the state where the second and the fourth to seventh switches are held in the OFF state as they are.

[0064] At this time, the current flows via the third switch, and the potential of the first node falls to a ground potential GND. For this reason, a voltage supplied to the electro-optical element becomes 0V, and the electro-optical element no longer emits light.

[0065] Next, in the state where the third switch is held in the ON state and the first and fifth switches are held in the OFF state as they are, the second, fourth, sixth, and seventh switches become ON.

[0066] Due to this, for example the predetermined potential 0V or an input potential  $V_{in}$  propagated through the data line is input to the second node, and the reference current flows in the third node by the reference current supplying means parallel to this. As a result, a gate/source voltage  $V_{gs}$  of the drive transistor is charged in the coupling capacitor element.

[0067] At this time, the drive transistor operates in the saturated region, therefore the gate/source voltage  $V_{gs}$  of the drive transistor becomes a term including a mobility  $\mu$  and a threshold value  $V_{th}$ . Further,  $V_0$  or  $V_{in}$  is charged in the pixel capacitor element at this time.

[0068] Next, the second and sixth switches become OFF. Due to this, the source potential of the drive transistor (potential of the third node) rises up to for example ( $V_0$  or  $V_{in} - V_{th}$ ).

[0069] Then, further, in the state where the third and seventh switches are held in the ON state, and the first, second, and sixth switches are held in the OFF state as they are, the fifth switch becomes ON, and the fourth switch becomes OFF. By the turning on of the fifth switch, the input voltage  $V_{in}$  propagated through the data line via the fifth switch couples a voltage  $\Delta V$  with the gate of the drive transistor through the coupling capacitor element.

[0070] This coupling amount  $\Delta V$  is determined according to a voltage change amount ( $V_{gs}$  of the drive transistor) between the first node and the second node, a pixel capacitor element, a coupling capacitor element, and a parasitic capacitance of the drive transistor, almost all of the change amount is coupled with the gate of the drive transistor if the capacitance of the coupling capacitor element is made large in comparison with the pixel capacitor element and the parasitic capacitance, and the gate potential of the drive transistor becomes  $V_0$  or ( $V_{in} + V_{gs}$ ).

[0071] After the end of the writing, the fifth and seventh switches become OFF, and further the first switch becomes ON and the third switch becomes OFF.

[0072] Due to this, the source potential of the drive transistor once falls to the ground potential GND, then rises, and the current starts to flow also in the electro-optical

element. Irrespective of the fact that the source potential of the drive transistor fluctuates, there is a pixel capacitor element between the gate and the source thereof. By making the capacitance of the pixel capacitor element larger than the parasitic capacitance of the drive transistor, the gate/source potential is always held at a constant value such as  $(V_{in} + V_{gs})$ .

[0073] At this time, the drive transistor is driven in the saturated region, therefore the value of the current  $I_{ds}$  flowing in the drive transistor becomes the value shown by Equation 1. That is determined by the gate/source voltage. This  $I_{ds}$  flows also in the electro-optical element in the same way, whereby the electro-optical element emits light.

#### EFFECT OF THE INVENTION

[0074] According to the present invention, even when the I-V characteristic of the EL light emitting element changes by aging, a source-follower output without luminance deterioration can be achieved.

[0075] A source-follower circuit of an n-channel transistor becomes possible, and an n-channel transistor can be used as a drive element of an EL light emitting element by using current anode/cathode electrodes as they are.

[0076] Further, not only the variation of threshold values of drive transistors, but also the variation of mobilities can be greatly suppressed, and image quality having good uniformity can be obtained.

[0077] Further, variation of the threshold values of drive transistors is cancelled out by the reference current, therefore it is not necessary to cancel the threshold value by setting the ON/OFF timing of the switch for each panel, therefore an increase of the number of steps for setting the timing can be suppressed.

[0078] Further, the capacitance inside the pixel can be easily designed, and the capacitance can be made smaller, therefore the pixel area can be reduced, and it becomes possible to make the definition of the panel higher.

[0079] Further, almost all of the voltage change can be coupled with the gate of the drive transistor when inputting the input voltage, therefore variation of the current value for each pixel can be reduced, and a uniform image quality can be obtained.

[0080] Further, the time during which the input voltage from the signal line is input into the pixel can be shortened by inputting the fixed potential to the gate of the drive transistor and sending the reference current  $I_{ref}$ , the data can be written into the pixel at a high speed, and it becomes possible to cope with a drive system dividing that 1 H into several parts and writing that data into the pixel as in a three-part write system.

[0081] Further, the transistors of the pixel circuits can be configured by only n-channel transistors, and it becomes able to use the a-Si process in TFT fabrication. Due to this, a reduction of the cost of the TFT substrate becomes possible.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0082] FIG. 1 is a block diagram showing the configuration of a general organic EL display device.

[0083] FIG. 2 is a circuit diagram showing an example of the configuration of the pixel circuit of FIG. 1.

[0084] FIG. 3 is a diagram showing aging of the current-voltage (I-V) characteristic of the organic EL element.

[0085] FIG. 4 is a circuit diagram showing a pixel circuit obtained by replacing a p-

channel TFT of the circuit of FIG. 2 by an n-channel TFT.

[0086] FIG. 5 is a diagram showing operation points of a drive transistor constituted by a TFT and an EL element in an initial state.

[0087] FIG. 6 is a diagram showing operation points of a drive transistor constituted by a TFT and an EL element after aging.

[0088] FIG. 7 is a circuit diagram showing a pixel circuit in which a source of the drive transistor constituted by an n-channel TFT is connected to a ground potential.

[0089] FIG. 8 is a block diagram showing the configuration of an organic EL display device employing a pixel circuit according to a first embodiment.

[0090] FIG. 9 is a circuit diagram showing a specific configuration of a pixel circuit according to the first embodiment in the organic EL display device of FIG. 8.

[0091] FIGS. 10A to 10I are timing charts for explaining a method of driving the circuit of FIG. 9.

[0092] FIGS. 11A and 11B are diagrams for explaining an operation according to the method of driving the circuit of FIG. 9.

[0093] FIGS. 12A and 12B are diagrams for explaining the operation according to the method of driving the circuit of FIG. 9.

[0094] FIG. 13 is a diagram for explaining the operation according to the method of driving the circuit of FIG. 9.

[0095] FIG. 14 is a diagram for explaining the operation according to the method of

driving the circuit of FIG. 9.

[0096] FIG. 15 is a diagram for explaining a reason why a reference current is supplied to the source of the drive transistor.

[0097] FIG. 16 is a diagram for explaining the reason why a reference current is supplied to the source of the drive transistor.

[0098] FIG. 17 is a diagram for explaining the reason why a reference current is supplied to the source of the drive transistor.

[0099] FIG. 18 is a diagram for explaining the reason why a reference current is supplied to the source of the drive transistor.

[0100] FIG. 19 is a circuit diagram showing a specific configuration of a pixel circuit according to a second embodiment.

[0101] FIGS. 20A to 20I are timing charts for explaining the method of driving the circuit of FIG. 19.

[0102] FIG. 21 is a block diagram showing the configuration of an organic EL display device employing a pixel circuit according to a third embodiment.

[0103] FIG. 22 is a circuit diagram showing a specific configuration of a pixel circuit according to a third embodiment in the organic EL display device of FIG. 21.

[0104] FIGS. 23A to 23H are timing charts for explaining the method of driving the circuit of FIG. 22.

[0105] FIG. 24 is a circuit diagram showing a specific configuration of the pixel circuit

according to a fourth embodiment.

[0106] FIGS. 25A to 25H are timing charts for explaining the method of driving the circuit of FIG. 24.

[0107] FIG. 26 is a circuit diagram showing a specific configuration of the pixel circuit according to a fifth embodiment.

[0108] FIG. 27 is a circuit diagram showing a specific configuration of the pixel circuit according to a sixth embodiment.

[0109] FIGS. 28A to 28K are timing charts for explaining the operation of the circuit of FIG. 26.

[0110] FIGS. 29A to 29K are timing charts of the circuit of FIG. 27.

[0111] FIGS. 30A and 30B are diagrams for explaining the operation of the circuit of FIG. 26.

[0112] FIGS. 31A and 31B are diagrams for explaining the operation of the circuit of FIG. 26.

[0113] FIGS. 32A and 32B are diagrams for explaining the operation of the circuit of FIG. 26.

[0114] FIGS. 33A and 33B are diagrams for explaining the operation of the circuit of FIG. 26.

[0115] FIG. 34 is a diagram for explaining the reason why the reference current is supplied to the source of the drive transistor in the circuit of FIG. 26.

[0116] FIG. 35 is a diagram for explaining the reason why the reference current is supplied to the source of the drive transistor in the circuit of FIG. 26.

[0117] FIG. 36 is a circuit diagram showing a specific configuration of the pixel circuit according to a seventh embodiment.

[0118] FIG. 37 is a circuit diagram showing a specific configuration of the pixel circuit according to an eighth embodiment.

[0119] FIGS. 38A to 38K are timing charts for explaining the operation of the circuit of FIG. 36.

[0120] FIGS. 39A to 39K are timing charts for explaining the operation of the circuit of FIG. 37.

[0121] FIG. 40 is a circuit diagram showing a specific configuration of the pixel circuit according to a ninth embodiment.

[0122] FIG. 41 is a circuit diagram showing a specific configuration of the pixel circuit according to a 10th embodiment.

[0123] FIGS. 42A to 42J are timing charts for explaining the operation of the circuit of FIG. 40.

[0124] FIGS. 43A to 43J are timing charts for explaining the operation of the circuit of FIG. 41.

[0125] FIG. 44 is a circuit diagram showing a specific configuration of the pixel circuit according to an 11th embodiment.

[0126] FIG. 45 is a circuit diagram showing a specific configuration of the pixel circuit according to a 12th embodiment.

[0127] FIGS. 46A to 46J are timing charts for explaining the operation of the circuit of FIG. 44.

[0128] FIGS. 47A to 47J are timing charts for explaining the operation of the circuit of FIG. 45.

[0129] In general, the reference numerals used refer to elements as described; 100, 100A to 100J . . . display device, 101 . . . pixel circuit (PXL), 102 . . . pixel array, 103 . . . horizontal selector (HSEL), 104 . . . write scanner (WSCN), 105 . . . first drive scanner (DSCN1), 106 . . . second drive scanner (DSCN2), 107 . . . third drive scanner (DSCN3), 108 . . . fourth drive scanner (DSCN4), 109 . . . fifth drive scanner (DSCN5), 110 . . . sixth drive scanner (DSCN6), DTL101 to DTL10n . . . data line, WSL101 to WSL10m . . . scanning lines, DSL101 to DSL10m, DSL111 to DSL11m, DSL121 to DSL12m, DSL131 to DSL13m, DSL141 to DSL14m, DSL151 to DSL15m, DSL161 to DSL16m . . . drive lines, 111 . . . drive transistor constituted by TFT, 112 . . . first switch constituted by TFT, 113 . . . second switch constituted by TFT, 114 . . . third switch constituted by TFT, 115 . . . fourth switch constituted by TFT, 116 . . . fifth switch constituted by TFT, 117 . . . sixth switch constituted by TFT, 118 . . . seventh switch constituted by TFT, 119 . . . light emitting element, 120 . . . seventh or eighth switch constituted by TFT, 121 . . . eighth or ninth switch constituted by TFT, ND111 . . . first node, ND112 . . . second node, ND113 . . . third node, ND114 . . . fourth node.

#### BEST MODE FOR WORKING THE INVENTION

[0130] Below, embodiments of the present invention will be explained with reference to the attached drawings.

#### First Embodiment

[0131] FIG. 8 is a block diagram showing the configuration of an organic EL display device employing a pixel circuit according to the first embodiment.

[0132] FIG. 9 is a circuit diagram showing a specific configuration of a pixel circuit according to the first embodiment in the organic EL display device of FIG. 8.

[0133] This display device 100, as shown in FIG. 8 and FIG. 9, has a pixel array 102 comprised of pixel circuits (PXLC) 101 arranged in an  $m \times n$  matrix, horizontal selector (HSEL) 103, write scanner (WSCN) 104, first drive scanner (DSCN1) 105, second drive scanner (DSCN2) 106, third drive scanner (DSCN3) 107, fourth drive scanner (DSCN4) 108, fifth drive scanner (DSCN5) 109, sixth drive scanner (DSCN6) 110, reference constant current source (RCIS) 111, data lines DTL101 to DTL10n selected by the horizontal selector 103 and supplied with data signals in accordance with the luminance information, scanning lines WSL101 to WSL10m selected and driven by the write scanner 104, drive lines DSL101 to DSL10m selected and driven by the first drive scanner 105, drive lines DSL111 to DSL11m selected and driven by the second drive scanner 106, drive lines DSL121 to DSL12m selected and driven by the third drive scanner 107, drive lines DSL131 to DSL13m selected and driven by the fourth drive scanner 108, drive lines DSL141 to DSL14m selected and driven by the fifth drive scanner 109, drive lines DSL151 to DSL15m selected and driven by the sixth drive scanner 110, and reference current supply lines ISL101 to ISL10n supplied with the reference current  $I_{ref}$  by the constant current source 111.

[0134] Note that, in the pixel array 102, the pixel circuits 101 are arranged in an  $m \times n$  matrix, but in FIG. 8, for simplification of the drawing, an example in which they are arranged in a  $2(=m) \times 3(=n)$  matrix is shown.

[0135] Further, in FIG. 9 as well, for simplification of the drawing, the specific configuration of one pixel circuit is shown.

[0136] The pixel circuit 101 according to the first embodiment, as shown in FIG. 9, has n-channel TFT 111 to TFT 118, capacitors C111 and C112, a light emitting element 119 made of an organic EL element (OLED: electro-optical element), a first node ND111, a second node ND112, a third node ND113, and a fourth node ND114.

[0137] Further, in FIG. 9, DTL101 indicates the data line, WSL101 indicates the scanning line, and DSL101, DSL111, DSL121, DSL131, DSL141, and DSL151 indicate drive lines.

[0138] Among these components, the TFT 111 configures the field effect transistor (drive transistor) according to the present invention, the TFT 112 configures the first switch, the TFT 113 configures the second switch, the TFT 114 configures the third switch, the TFT 115 configures the fourth switch, the TFT 116 configures the fifth switch, the TFT 117 configures the sixth switch, the TFT 118 configures the seventh switch as the electric connecting means, the capacitor C111 configures the pixel capacitor element according to the present invention, and the capacitor C112 configures the coupling capacitor element according to the present invention.

[0139] The supply line (power supply potential) of the power supply voltage VCC corresponds to the first reference potential, and the ground potential GND corresponds to the second reference potential.

[0140] Further, in the first embodiment, the data line and the predetermined potential line are shared.

[0141] In the pixel circuit 101, between the first reference potential (the power supply potential VCC in the present embodiment) and the second reference potential (the ground

potential GND in the present embodiment), the drive transistor constituted by the TFT 111, the third node ND113, the first switch constituted by the TFT 112, the first node ND111, and the light emitting element (OLED) 119 are connected in series.

[0142] Specifically, a cathode of the light emitting element 119 is connected to the ground potential GND, an anode is connected to the first node ND111, the source of the TFT 112 is connected to the first node ND111, source and drain of the TFT 112 are connected between the first node ND111 and the third node ND113, a source of the TFT 111 is connected to the third node ND113, and a drain of the TFT 111 is connected to the power supply potential VCC.

[0143] A gate of the TFT 111 is connected to the second node ND112, and a gate of the TFT 112 is connected to the drive line DSL111 driven by the second drive scanner 106.

[0144] A source and drain of the second switch constituted by the TFT 113 are connected between the third node ND113 and the fourth node ND114, and a gate of the TFT 113 is connected to the drive line DSL141 driven by the fifth drive scanner 109.

[0145] A drain of the third switch constituted by the TFT 114 is connected to the first node ND111 and a first electrode of the capacitor C111, a source is connected to the fixed potential (the ground potential GND in the present embodiment), and a gate of the TFT 114 is connected to the drive line DSL151 driven by the sixth drive scanner. Further, a second electrode of the capacitor C111 is connected to the second node ND112.

[0146] A source and drain of the seventh switch constituted by the TFT 118 are connected to the second node ND112 and a first electrode of the capacitor C112, and a gate driven by the third drive scanner of the TFT 118 is connected to the drive line DSL121.

[0147] A source and drain of the fourth switch constituted by the TFT 115 are connected

to the data line (predetermined potential line) DTL101 and the second node ND112, and a gate of the TFT 115 is connected to the drive line DSL131 driven by the fourth drive scanner 108.

[0148] A source and drain of the fifth switch constituted by the TFT 116 are connected to the data line DTL101 and the fourth node ND114. A gate of the TFT 116 is connected to the scanning line WSL101 driven by the write scanner 104.

[0149] Further, the source and drain of the sixth switch constituted by the TFT 117 are connected between the third node ND113 and the reference current supply source line ISL101. A gate of the TFT 117 is connected to the drive line DSL101 driven by the first drive scanner 105.

[0150] In this way, the pixel circuit 101 according to the present embodiment is configured so that the pixel capacitance constituted by the capacitor C111 is connected between the gate and source of the drive transistor constituted by the TFT 111, a source side potential of the TFT 111 is connected to the fixed potential via the switch transistor constituted by the TFT 114 in a non-light emission period, the predetermined reference current (for example  $2\ \mu\text{A}$ ) is supplied to the source of the TFT 111 (third node ND13) at a predetermined timing, a voltage corresponding to the reference current  $I_{\text{ref}}$  is held, and the input signal voltage is coupled centered on the voltage, whereby the EL light emitting element 119 is driven centered about the center value of variations of the mobilities, and an image quality suppressing the variation of the uniformity due to variation of the mobilities of the drive transistor constituted by the TFT 111 is obtained.

[0151] Next, the operation of the above configuration will be explained focusing on the operation of the pixel circuit with reference to FIGS. 10A to 10I and FIG. 11, FIGS. 12A and 12B, and FIG. 13 and FIG. 14.

[0152] Note that FIG. 10A shows a drive signal  $ds[4]$  applied to the drive line DSL131 of

the first row in the pixel alignment, FIG. 10B shows a scanning signal  $ws[1]$  applied to the scanning line WSL101 of the first row in the pixel alignment, FIG. 10C shows a drive signal  $ds[3]$  applied to the drive line DSL121 of the first row in the pixel alignment, FIG. 10D shows a drive signal  $ds[5]$  applied to the drive line DSL141 of the first row in the pixel alignment, FIG. 10E shows a drive signal  $ds[6]$  applied to the drive line DSL151 of the first row in the pixel alignment, FIG. 10F shows a drive signal  $ds[2]$  applied to the drive line DSL111 of the first row in the pixel alignment, FIG. 10G shows a drive signal  $ds[1]$  applied to the drive line DSL101 of the first row in the pixel alignment, FIG. 10H shows a gate potential  $Vg111$  of the drive transistor constituted by the TFT 111, and FIG. 10I shows a potential  $VND111$  of the first node ND111.

[0153] First, at the time of the light emission state of the ordinary EL light emitting element 119, as shown in FIGS. 10A to 10G, the scanning signal  $ws[1]$  to the scanning line WSL101 is set at the low level by the write scanner 104, the drive signal  $ds[1]$  to the drive line DSL101 is set at the low level by the drive scanner 105, the drive signal  $ds[3]$  to the drive line DSL121 is set at the low level by the drive scanner 107, the drive signal  $ds[4]$  to the drive line DSL131 is set at the low level by the drive scanner 108, the drive signal  $ds[5]$  to the drive line DSL141 is set at the low level by the drive scanner 109, the drive signal  $ds[6]$  to the drive line DSL151 is set at the low level by the drive scanner 110, and only the drive signal  $ds[2]$  to the drive line DSL111 is selectively set at a high level by the drive scanner 106.

[0154] As a result, in the pixel circuit 101, as shown in FIG. 11A, the TFT 112 is held in the ON state (conductive state), and the TFT 113 to TFT 118 are held in the OFF state (non-conductive state).

[0155] The drive transistor 111 is designed so as to operate in the saturated region, and the current  $I_{ds}$  flowing in the EL light emitting element 119 takes a value shown by the above Equation 1.

[0156] Next, in the non-light emission period of the EL light emitting element 119, as shown in FIGS. 10A to 10G, the scanning signal ws[1] to the scanning line WSL101 is held at the low level by the write scanner 104, the drive signal ds[1] to the drive line DSL101 is held at the low level by the drive scanner 105, the drive signal ds[2] to the drive line DSL111 is switched to the low level by the drive scanner 106, the drive signal ds[3] to the drive line DSL121 is held at the low level by the drive scanner 107, the drive signal ds[4] to the drive line DSL131 is held at the low level by the drive scanner 108, the drive signal ds[5] to the drive line DSL141 is held at the low level by the drive scanner 109, and the drive signal ds[6] to the drive line DSL151 is selectively set at the high level by the drive scanner 110.

[0157] As a result, in the pixel circuit 101, as shown in FIG. 11B, the TFT 112 becomes OFF, and the TFT 114 becomes ON in the state where the TFT 113, and TFT 115 to TFT 118 are held in the OFF state as they are.

[0158] At this time, the current flows via the TFT 114, and the potential VND111 of the first node ND111 falls to the ground potential GND as shown in FIGS. 10H and 10I. For this reason, the voltage applied to the EL light emitting element 119 becomes 0V, and the EL light emitting element 119 no longer emits light.

[0159] Next, as shown in FIGS. 10A to 10G, in the state where the scanning signal ws[1] to the scanning line WSL101 is held at the low level by the write scanner 104, the drive signal ds[2] to the drive line DSL111 is held at the low level by the drive scanner 106, and the drive signal ds[6] to the drive line DSL151 is held at the high level by the drive scanner 110, the drive signal ds[1] to the drive line DSL101 from the drive scanner 105, the drive signal ds[3] to the drive line DSL121 by the drive scanner 107, the drive signal ds[4] to the drive line DSL131 by the drive scanner 108, and the drive signal ds[5] to the drive line DSL141 are selectively set at the high level by the drive scanner 109.

[0160] As a result, in the pixel circuit 101, as shown in FIG. 12A, the TFT 113, TFT 115,

TFT 117, and TFT 118 become ON in the state where the TFT 114 is held in the ON state and the TFT 112 and 116 are held in the OFF state as they are.

[0161] Due to this, the input voltage  $V_{in}$  propagated through the data line DTL101 via the TFT 115 is input to the second node ND112, and the reference current  $I_{ref}$  (for example  $2 \mu A$ ) supplied to the reference current supply line ISL101 by the constant current source 111 flows in the third node ND113 parallel to this. As a result, the voltage  $V_{gs}$  between the gate and source of the drive transistor constituted by the TFT 111 is charged in the capacitor C112.

[0162] At this time, the TFT 111 operates in the saturated region, therefore, as shown in the following Equation (2), the gate/source voltage  $V_{gs}$  of the TFT 111 becomes a term including the mobility  $\mu$  and the threshold value  $V_{th}$ . Further, at this time,  $V_{in}$  is charged in the capacitor C111.

[0163] (Equation 2)  $V_{gs} = V_{th} + \{2I_{ds} / (\mu (W/L)C_{ox})\}^2$  (2)

[0164] Next, after  $V_{in}$  is charged in the capacitor C111, as shown in FIGS. 10A to 10G, in the state where the scanning signal  $ws[1]$  to the scanning line WSL101 is held at the low level by the write scanner 104, the drive signal  $ds[2]$  to the drive line DSL111 is held at the low level by the drive scanner 106, the drive signal  $ds[3]$  to the drive line DSL121 is held at the high level by the drive scanner 107, the drive signal  $ds[4]$  to the drive line DSL131 is held at the high level by the drive scanner 108, and the drive signal  $ds[6]$  to the drive line DSL151 is held at the high level by the drive scanner 110, the drive signal  $ds[1]$  to the drive line DSL101 is selectively set at the low level by the drive scanner 105, and the drive signal  $ds[4]$  to the drive line DSL141 is selectively set at the low level by the drive scanner 109.

[0165] As a result, in the pixel circuit 101, from the state of FIG. 12A, the TFT 113 and the TFT 117 become OFF. Due to this, the source potential of the TFT 111 (potential of

the third node ND113) rises up to  $(V_{in}-V_{th})$ .

[0166] Then, further, the scanning signal  $ws[1]$  to the scanning line WSL101 is switched to the high level by the write scanner 104, and the drive signal  $ds[4]$  to the drive line DSL131 is switched to the low level by the drive scanner 108.

[0167] As a result, in the pixel circuit 101, as shown in FIG. 12B, in the state where the TFT 114 and the TFT 118 are held in the ON state, and the TFT 112, the TFT 113, and the TFT 117 are held in the OFF state as they are, the TFT 116 becomes ON, and the TFT 115 becomes OFF.

[0168] By the turning on of the TFT 116, the input voltage  $V_{in}$  propagated through the data line DTL101 via the TFT 116 couples the voltage  $\Delta V$  with the gate of the TFT 111 through the capacitor C112.

[0169] This coupling amount  $\Delta V$  is determined according to the voltage change between the first node ND111 and the second node ND112 ( $V_{gs}$  of the TFT 111), capacitances of capacitors C111 and C112, and the parasitic capacitance 113 of the TFT 111. When the capacitance of the capacitor C112 is made large in comparison with the capacitance of the capacitor C111 and the parasitic capacitance C113, almost all of the change is coupled with the gate of the TFT 111, and the gate potential of the TFT 111 becomes  $(V_{in}+V_{gs})$ .

[0170] After the end of the writing, as shown in FIGS. 10A to 10G, the scanning signal  $ws[1]$  to the scanning line WSL101 is switched to the low level by the write scanner 104, the drive signal  $ds[3]$  to the drive line DSL121 is switched to the low level by the drive scanner 107, further the drive signal  $ds[2]$  to the drive line DSL111 is switched to the high level by the drive scanner 106, and the drive signal  $ds[6]$  to the drive line DSL151 is switched to the low level by the drive scanner 110.

[0171] Due to this, in the pixel circuit 101, as shown in FIG. 13, the TFT 116 and the TFT 118 become OFF, and further the TFT 112 becomes ON, and the TFT 114 becomes OFF.

[0172] Due to this, the source potential of the TFT 111 once falls to the ground potential GND then rises, and current starts to flow also in the EL light emitting element 119. Irrespective of the fluctuation of the source potential of the TFT 111, the capacitor C111 exists between the gate and source thereof. By making the capacitance of the capacitor C111 larger than the parasitic capacitance C113 of the TFT 111, the gate/source potential is constantly held at the constant value such as  $(V_{in} + V_{gs})$ .

[0173] At this time, the TFT 111 is driven in the saturated region, therefore the value of the current  $I_{ds}$  flowing in the TFT 111 becomes the value shown by Equation 1 and is determined by the gate/source voltage. This  $I_{ds}$  flows also in the EL light emitting element 119 in the same way, and the EL light emitting element 119 emits light.

[0174] An equivalent circuit of the pixel circuit 101 including this EL light emitting element 119 becomes as shown in FIG. 14, therefore the source potential of the TFT 111 rises up to the gate potential for running the current  $I_{ds}$  through the EL light emitting element 119. Along with this potential rise, the gate potential of the TFT 111 rises in the same way via the capacitor C111.

[0175] Due to this, the gate/source potential of the TFT 111 is held constant as previously explained.

[0176] Here, the reference current  $I_{ref}$  will be considered.

[0177] As explained above, by running the reference current  $I_{ref}$ , the gate/source voltage of the TFT 111 is given the value represented by Equation 2.

[0178] However, the gate/source voltage does not become  $V_{th}$  when  $I_{ref}=0$ . This is because even when the gate/source voltage becomes  $V_{th}$ , a leakage current slightly flows in the TFT 111, therefore, as shown in FIG. 15, the source voltage of the TFT 111 rises up to  $V_{cc}$ .

[0179] In order to make the gate/source voltage of the TFT 111  $V_{th}$ , it is necessary to adjust the period for turning on the TFT 113 and turn off the TFT 113 when the gate/source voltage becomes  $V_{th}$ . This timing must be adjusted for each panel in a real device.

[0180] As in the present embodiment, when the reference current  $I_{ref}$  is not flowing, even if the gate/source voltage can be set at  $V_{th}$  by adjusting the timing of the TFT 113, even when the same input voltage  $V_{in}$  is applied in for example the pixels A and B having different mobilities, according to Equation 1, variation of the current  $I_{ds}$  occurs according to the mobility  $\mu$  as shown in FIG. 16, and the luminance of the pixel becomes different. That is, as a larger value of current flows and it becomes brighter, the current value is affected by the variation of mobilities, the uniformity varies, and the image quality is degraded.

[0181] However, as in the present embodiment, by running a constant amount of reference current  $I_{ref}$ , as shown in FIG. 17, not according to the ON/OFF timing of the TFT 113, the gate/source voltage of the TFT 111 can be set to a constant value shown in Equation 2. Even in the pixels A and B having different mobilities, as shown in FIG. 18, the variation of the current  $I_{ds}$  can be kept small, therefore variation of the uniformity can be suppressed.

[0182] Further, the circuit of the present embodiment will be considered based on problems of the usual source-follower. Also in the present circuit, as the light emission time of the EL light emitting element 119 becomes longer, the I-V characteristic thereof deteriorates. For this reason, even when the TFT 111 passes the same value of current,

the potential applied to the EL light emitting element 119 changes, and the potential VND111 of the first node ND111 falls.

[0183] However, in the present circuit, the potential VND111 of the first node ND111 falls in the state where the gate/source potential of the TFT 111 is held constant as it is, therefore the current flowing in the TFT 111 does not change.

[0184] Accordingly, even when the current flowing in the EL light emitting element 119 does not change, and the I-V characteristic of the EL light emitting element 119 deteriorates, a current corresponding to the gate/source voltage constantly continuously flows, so the past problems can be solved.

[0185] As explained above, according to the first embodiment, the voltage drive type TFT active matrix organic EL display device is configured so that the capacitor C111 is connected between the gate and source of the drive transistor constituted by the TFT 111, the source side of the TFT 111 (the first node ND111) is connected through the TFT 114 to the fixed potential (GND in the present embodiment), the predetermined reference current (for example  $2\ \mu\text{A}$ )  $I_{\text{ref}}$  is supplied to the source of the TFT 111 (the third node ND13) at a predetermined timing, the voltage corresponding to the reference current  $I_{\text{ref}}$  is held, and the input signal voltage is coupled centered about the voltage, to thereby drive the EL light emitting element 119 centered about the center value of variations of mobilities, therefore the following effects can be obtained.

[0186] Namely, even when the I-V characteristic of the EL light emitting element changes by aging, a source-follower output without luminance deterioration can be obtained.

[0187] A source-follower circuit of an n-channel transistor becomes possible, and the n-channel transistor can be used as the drive element of the EL light emitting element by using current anode/cathode electrodes as they are.

[0188] Further, not only variation of threshold values of drive transistors, but also variation of mobilities can be greatly suppressed, and an image quality having good uniformity can be obtained.

[0189] Further, variation of the threshold values of drive transistors is cancelled out by the reference current, therefore it is not necessary to cancel the threshold value by setting the ON/OFF timing of the switch for each panel, therefore an increase of the number of steps for setting the timing can be suppressed.

[0190] Further, the transistors of the pixel circuits can be configured by only n-channel transistors, and it becomes able to use the a-Si process in TFT fabrication. Due to this, a reduction of the cost of the TFT substrate becomes possible.

#### Second Embodiment

[0191] FIG. 19 is a circuit diagram showing the specific configuration of a pixel circuit according to a second embodiment. Further, FIG. 20 is a timing chart of the circuit of FIG. 19.

[0192] The difference of the second embodiment from the first embodiment explained above resides in that the fourth switch constituted by the TFT 115 does not share the predetermined potential line to which the TFT 115 is connected together with the data line DTL, but is separately provided.

[0193] The rest of the configuration is the same as that of the first embodiment, so a detailed explanation concerning the configuration and function is omitted here.

[0194] In the second embodiment, when running the reference current  $I_{ref}$  to the source of the driver transistor constituted by the TFT 111, the input voltage  $V_{in}$  is not input to

the gate voltage of the TFT 111, but the fixed potential V0 is input. By inputting the fixed potential V0 and running the reference current Iref, the time during which the Vin is input into the pixel can be shortened, and the data can be written into the pixel at a high speed.

[0195] For this reason, it becomes possible to cope with a drive system dividing that 1 H into several parts and writing that data into the pixel as in a three-part write system.

### Third Embodiment

[0196] FIG. 21 is a block diagram showing the configuration of an organic EL display device employing a pixel circuit according to a third embodiment.

[0197] FIG. 22 is a circuit diagram showing the specific configuration of a pixel circuit according to the third embodiment in the organic EL display device of FIG. 21. Further, FIGS. 23A to 23H are timing charts of the circuit of FIG. 22.

[0198] The difference of the third embodiment from the first embodiment resides in that, in place of the configuration in which the electric connecting means for connecting the first electrode of the capacitor C112 and the second node ND112 is configured by the switch 118 for selectively connecting the two, they are directly connected by an electric interconnect.

[0199] As a result, the third drive scanner 107 and the drive line DSL121 become unnecessary.

[0200] The rest of the configuration is the same as that of the second embodiment explained above.

[0201] According to the third embodiment, in addition to the effects of the first embodiment explained above, there are the advantages that the number of elements in the

pixel circuit can be decreased, and the circuit configuration can be simplified.

#### Fourth Embodiment

[0202] FIG. 24 is a circuit diagram showing a specific configuration of the pixel circuit according to the fourth embodiment. Further, FIGS. 25A to 25H are timing charts of the circuit of FIG. 24.

[0203] The difference of the fourth embodiment from the third embodiment explained above resides in that the predetermined potential line to which the TFT 115 as the fourth switch is connected is not shared together with the data line DTL, but is separately provided.

[0204] The rest of the configuration is the same as that of the first embodiment, so a detailed explanation concerning the configuration and function is omitted here.

[0205] In the fourth embodiment, when running the reference current  $I_{ref}$  to the source of the driver transistor constituted by the TFT 111, the input voltage  $V_{in}$  is not input to the gate voltage of the TFT 111, but the fixed potential  $V_0$  is input. By inputting the fixed potential  $V_0$  and running the reference current  $I_{ref}$ , the time during which the  $V_{in}$  is input into the pixel can be shortened, and the data can be written into the pixel at a high speed.

[0206] For this reason, it becomes possible to cope with a drive system dividing that 1 H into several parts and writing that data into the pixel as in a three-part write system.

#### Fifth Embodiment and Sixth Embodiment

[0207] FIG. 26 is a circuit diagram showing the specific configuration of a pixel circuit according to a fifth embodiment. Further, FIG. 27 is a circuit diagram showing a specific configuration of the pixel circuit according to a sixth embodiment.

[0208] The difference of the fifth embodiment from the first embodiment explained above resides in that an eighth switch constituted by a TFT 120 is inserted between the first node ND111 and the anode of the light emitting element 119, the first node ND111 and the data line DTL101 are connected by a ninth switch constituted by a TFT 121, and the source of the TFT 114 is connected to the fixed potential V0.

[0209] A gate of the TFT 120 is connected to drive lines DSL161 (to 16m) driven by a seventh drive scanner (DSCN7) 122, and a gate of the TFT 121 is connected to drive lines DSL171 (to 17m) driven by an eighth drive scanner (DSCN8) 123.

[0210] Further, the difference of the sixth embodiment from the fifth embodiment resides in that the first node ND111 is selectively connected to the fourth node ND114 in place of selectively connecting the first node ND111 to the data line DTL101 by the TFT 121.

[0211] Basically, the same operation is carried out in the fifth and sixth embodiments.

[0212] FIGS. 28A to 28K and FIGS. 29A to 29K show timing charts of examples of those operations.

[0213] Note that FIG. 28A and FIG. 29A show the drive signal ds[4] applied to the drive line DSL131 of the first row in the pixel alignment, FIG. 28B and FIG. 29B show the scanning signal ws[1] applied to the scanning line WSL101 of the first row in the pixel alignment, FIG. 28C and FIG. 29C show the drive signal ds[3] applied to the drive line DSL121 of the first row in the pixel alignment, FIG. 28D and FIG. 29D show the drive signal ds[5] applied to the drive line DSL141 of the first row in the pixel alignment, FIG. 28E and FIG. 29E show the drive signal ds[2] applied to the drive line DSL111 of the first row in the pixel alignment, FIG. 28F and FIG. 29F show the drive signal ds[1] applied to the drive line DSL101 of the first row in the pixel alignment, FIG. 28G and FIG. 29G show the drive signal ds[7] applied to the drive line DSL161 of the first row in

the pixel alignment, FIG. 28H and FIG. 29H show the drive signal  $ds[6]$  applied to the drive line DSL141 of the first row in the pixel alignment, FIG. 28I and FIG. 29I show the drive signal  $ds[8]$  applied to the drive line DSL171 of the first row in the pixel alignment, FIG. 28J and FIG. 29J show the gate potential  $V_{g111}$  of the TFT 111 as the drive transistor, and FIG. 28K and FIG. 29K show the potential  $V_{ND111}$  of the first node ND111.

[0214] Below, the operation of the circuit of FIG. 26 will be explained with reference to FIGS. 30A and 30B, FIGS. 31A and 31B, FIGS. 32A and 32B, and FIGS. 33A and 33B.

[0215] First, the light emission state of the ordinary EL light emitting element 119 is the state where the TFT 112 and the TFT 120 become ON as shown in FIG. 30A.

[0216] Next, in the non-light emission period of the EL light emitting element 119, as shown in FIG. 30B, the TFT 120 is turned off while turning on the TFT 112 as it is.

[0217] At this time, a current is no longer supplied to the EL light emitting element 119, so it no longer emits the light.

[0218] Next, as shown in FIG. 31A, the TFT 115, TFT 118, TFT 113 and TFT 117 are turned on and the input voltage ( $V_{in}$ ) is input to the gate of the drive transistor constituted by the TFT 111. By running the current  $I_{ref}$  from the current source, the gate/source voltage  $V_{gs}$  of the drive transistor is charged in the capacitors C111 and C112. At this time, the TFT 114 operates in the saturated region, therefore  $V_{gs}$  becomes a term including  $\mu$  and  $V_{th}$  as shown in Equation 3.

[0219] (Equation 3)  $V_{gs} = V_{th} + [2I / (\mu (W/L)C_{ox})]^{1/2} \quad \dots(3)$

[0220] After  $V_{gs}$  is charged in the capacitors C111 and C112, the TFT 113 and TFT 112 are turned off. Due to this, the voltages charged in the capacitors C111 and C112 are set

to  $V_{gs}$ .

[0221] Thereafter, as shown in FIG. 31B, by turning off the TFT 117 and suspending the supply of the current, the source potential of the TFT 111 rises up to  $V_{in}-V_{th}$ .

[0222] Further, as shown in FIG. 32A, the TFT 115 is turned off and the TFT 116 and TFT 121 are turned on.

[0223] By turning on the TFT 116 and TFT 121,  $V_{in}$  is passed through the capacitors C111 and C112 and the voltage  $\Delta V$  is coupled with the gate of the drive transistor constituted by the TFT 111. This coupling amount  $\Delta V$  is determined according to the voltage change ( $V_{gs}$ ) of a point A and a point B in the figure and a ratio of a sum of capacitances C1 and C2 of the capacitors C111 and C112 and the parasitic capacitance C3 of the TFT 111 (Equation 4). When the sum of C1 and C2 is made larger than C3, almost all of the change is coupled with the gate of the TFT 111, and the gate potential of the TFT 111 becomes  $V_{in}+V_{gs}$ .

[0224] (Equation 4)  $\Delta V = \Delta V_1 + \Delta V_2 = \{(C1+C2)/(C1+C2+C3)\} \cdot V_{gs} \quad \dots(4)$

[0225] After the writing ends, as shown in FIG. 32B, the TFT 121 is turned off and the TFT 114 is turned on.

[0226] The TFT 114 is connected to a fixed potential such as  $V_0$ . By turning on it, the voltage change ( $V_0-V_{in}$ ) of the node ND112 is coupled with the gate of the TFT 111 through the capacitor C111 again. This coupling amount  $\Delta V_3$  is determined according to voltage change of the node ND112 and the ratio of the sum of C1 and C3 and C2 (Equation 5). When defining this ratio as  $\alpha$ , the gate potential of the TFT 111 becomes  $(1-\alpha)V_{in}+V_{gs}+\alpha V_0$ , and the voltage held in the capacitor C111 rises from  $V_{gs}$  by exactly  $(1-\alpha)(V_{in}-V_0)$ .

[0227] (Equation 5)  $\Delta V = \{C1/(C1+C2+C3)\} \cdot (V_0 - V_{in}) = \alpha \quad \dots(5)$

[0228] Thereafter, as shown in FIG. 33A, the TFT 116 and TFT 118 are turned off, the TFT 112 and TFT 120 are turned on, and the TFT 114 is turned off. Due to this, the source potential of the TFT 111 once becomes the  $V_0$  level, then current starts to flow in the EL light emitting element 119. Irrespective of the fact that the source potential of the TFT 111 fluctuates, the capacitor C111 exists between the gate and the source. By making the capacitance C1 of the capacitor C111 larger than the parasitic capacitance C3, the gate/source potential is constantly held at a constant value.

[0229] At this time, the TFT 111 is driven in the saturated region, therefore the value of current  $I_{ds}$  flowing in the TFT 111 becomes the value indicated by Equation 1 and is determined by the gate/source voltage. This  $I_{ds}$  flows also in the EL light emitting element 119 in the same way, and the EL light emitting element 119 emits light.

[0230] The equivalent circuit of the element becomes as shown in FIG. 33B, therefore the source voltage of the TFT 111 rises up to the gate potential for running the current  $I_{ds}$  through the EL light emitting element 119. Along with this potential rise, the gate potential of the TFT 111 rises in the same way via the capacitor C111. Due to this, the gate/source voltage is held constant as previously explained, the EL light emitting element 119 is deteriorated by aging, therefore even when the source potential of the TFT 111 changes, the gate/source voltage is constant as it is, and the value of current flowing in the EL light emitting element 119 will not change.

[0231] Here, the capacitances C1 and C2 of the capacitors C111 and C112 will be considered.

[0232] First, the sum of C1 and C2 must be set to  $C1+C2 \gg C3$ . By making the sum much larger than C3, all of the potential change of the nodes ND111 and ND112 can be coupled with the gate of the TFT 111.

[0233] At this time, the value of current flowing through the TFT 111 becomes the value shown by Equation 1, the gate/source voltage of the TFT 111 becomes larger than the voltage flowing through the  $I_{ref}$  by exactly a constant value such as  $\alpha (V_0 - V_{in})$  as in FIG. 34, and even in pixels A and B having different mobilities, the variation of  $I_{ds}$  can be suppressed to small, therefore the variation of the uniformity can be suppressed.

[0234] However, when  $C_1 + C_2$  is made small, all of the voltage change of the nodes ND111 and ND112 is not coupled, but a gain ends up occurring. When this gain is defined as  $\beta$ , the amount of current flowing in the TFT 111 is represented by Equation 6, and the gate/source voltage of T10 becomes larger than the voltage for sending  $I_{ref}$  by exactly a value such as  $V_{in} + (\beta - 1)V_{gs}$ , but  $V_{gs}$  has a different value for each pixel, therefore it becomes unable to keep variation of the  $I_{ds}$  small (FIG. 35). Due to this,  $C_1 + C_2$  must be made larger than  $C_3$ .

[0235] (Equation 6)  $\Delta V = \{C_1 / (C_1 + C_2 + C_3)\} \cdot V_{gs} \quad \dots(6)$

[0236] Next, the magnitude of  $C_1$  will be considered.

[0237]  $C_1$  must be much larger than the parasitic capacitance  $C_3$ . If  $C_1$  is at the same level as  $C_3$ , the fluctuation of the source potential of the TFT 114 is coupled with the gate of the TFT 114 through the capacitor  $C_{111}$ , and the voltage held in the capacitor  $C_{111}$  fluctuates. For this reason, the TFT 111 becomes unable to carry a constant amount of current, and variation occurs for each pixel. Due to this,  $C_1$  must be made very large in comparison with the parasitic capacitance  $C_3$  of the TFT 111.

[0238] Further,  $C_2$  will be considered. Assuming that  $C_2 \gg C_1$ , when turning on the TFT 114 and coupling the voltage change such as  $V_0 - V_{in}$  with the gate of the TFT 111 through the capacitor  $C_{111}$ , the potential difference held in the capacitor  $C_{111}$  increases from the potential such as  $V_{gs}$  held by running  $I_{ref}$  through the TFT 111 by exactly a

constant value such as  $V_{in}-V_0$ , therefore, even in the pixels A and B having different mobilities, the variation of  $I_{ds}$  can be kept small, and variation of the uniformity can be suppressed.

[0239] However, assuming that  $C_2 \gg C_1$ , the variation of  $I_{ds}$  cannot be kept small, and also variation of the uniformity cannot be suppressed.

[0240] Next, if  $C_2 \ll C_1$ , when turning on the TFT 114, the voltage change such as  $V_0-V_{in}$  is completely coupled with the gate of the TFT 111 through the capacitor C111, therefore the voltage held in the capacitor C111 does not change at all from  $V_{gs}$ . Due to this, the EL light emitting element 119, irrespective of the input voltage, can only carry a constant current such as  $I_{ref}$ , therefore the pixel can only perform raster display.

[0241] Due to the above, it is necessary to set the magnitudes of C1 and C2 at the same level and impart a constant gain in the coupling by turning on the TFT 114.

[0242] Here, as previously explained, C3 is the parasitic capacitance of the TFT 114, and the magnitude thereof is an order of several tens to several hundreds of fF, but the relationships of C1, C2, and C3 are  $C_2 \gg C_3$  and  $C_1 \gg C_3$ , and C1 and C2 must be the same level, therefore C1 and C2 may have magnitudes of from several hundreds fF to several pF. Due to this, the capacitance can be easily set in a limited magnitude inside the pixel, and also the conventional problems of the current value varying for each pixel and unevenness of pixels occurring can be overcome.

#### Seventh Embodiment and Eighth Embodiment

[0243] FIG. 36 is a circuit diagram showing the specific configuration of a pixel circuit according to a seventh embodiment. FIG. 37 is a circuit diagram showing the specific configuration of a pixel circuit according to an eighth embodiment.

[0244] The difference of the seventh embodiment from the fifth embodiment explained above resides in that the predetermined potential line to which the fourth switch constituted by the TFT 115 is connected is not shared together with the data line DTL, but is separately provided.

[0245] In the same way, the difference of the eighth embodiment from the sixth embodiment explained above resides in that the predetermined potential line to which the fourth switch constituted by the TFT 115 is connected is not shared together with the data line DTL, but is separately provided.

[0246] The rests of the configurations are the same as those of the fifth and sixth embodiments, so a detailed explanation concerning the configurations and functions is omitted here.

[0247] The seventh and eighth embodiments basically operate in the same way.

[0248] FIGS. 38A to 38K and FIGS. 39A to 39K show timing charts of examples of those operations.

[0249] In the seventh and eighth embodiments, when running the reference current  $I_{ref}$  to the source of the driver transistor constituted by the TFT 111, the input voltage  $V_{in}$  is not input to the gate voltage of the TFT 111, but the fixed potential  $V_0$  is input. By inputting the fixed potential  $V_0$  and running the reference current  $I_{ref}$ , the time during which the  $V_{in}$  is input into the pixel can be shortened, and the data can be written into the pixel at a high speed.

[0250] For this reason, it becomes possible to cope with a drive system dividing that 1 H into several parts and writing that data into the pixel as in three-part write system.

Ninth Embodiment and 10th Embodiment

[0251] FIG. 40 is a circuit diagram showing the specific configuration of a pixel circuit according to a ninth embodiment. FIG. 41 is a circuit diagram showing the specific configuration of a pixel circuit according to a 10th embodiment.

[0252] The difference of the ninth embodiment from the fifth embodiment resides in that, in place of the configuration in which the electric connecting means for connecting the first electrode of the capacitor C112 and the second node ND112 is configured by the switch 118 for selectively connecting the two, they are directly connected by an electric interconnect.

[0253] The difference of the 10th embodiment from the sixth embodiment resides in that, in place of the configuration in which the electric connecting means for connecting the first electrode of the capacitor C112 and the second node ND112 is configured by the switch 118 for selectively connecting the two, they are directly connected by an electric interconnect.

[0254] As a result, the third drive scanner 107 and the drive line DSL121 become unnecessary.

[0255] The rests of the configurations are the same as those of the fifth and sixth embodiments explained above.

[0256] The ninth and 10th embodiments basically operate in the same way.

[0257] FIGS. 42A to 42J and FIGS. 43A to 43J show timing charts of examples of those operations.

[0258] According to the ninth and 10th embodiments, in addition to the effects of the fifth and sixth embodiments explained above, there are the advantages that the number of

elements in the pixel circuit can be decreased, and the circuit configuration can be simplified.

#### 11th Embodiment and 12th Embodiment

[0259] FIG. 44 is a circuit diagram showing the specific configuration of a pixel circuit according to an 11th embodiment. FIG. 45 is a circuit diagram showing the specific configuration of a pixel circuit according to a 12th embodiment.

[0260] The difference of the 11th embodiment from the seventh embodiment resides in that, in place of the configuration in which the electric connecting means for connecting the first electrode of the capacitor C112 and the second node ND112 is configured by the switch 118 for selectively connecting the two, they are directly connected by an electric interconnect.

[0261] The difference of the 12th embodiment from the eighth embodiment resides in that, in place of the configuration in which the electric connecting means for connecting the first electrode of the capacitor C112 and the second node ND112 is configured by the switch 118 for selectively connecting the two, they are directly connected by an electric interconnect.

[0262] As a result, the third drive scanner 107 and the drive line DSL121 become unnecessary.

[0263] The rest of the configurations are the same as those of the seventh and eighth embodiments explained above.

[0264] The 11th and 12th embodiments basically operate in the same way.

[0265] FIGS. 46A to 46J and FIGS. 47A to 47J show timing charts of examples of those

operations.

[0266] According to the 11th and 12th embodiments, in addition to the effects of the seventh and eighth embodiments explained above, there are the advantages that the number of elements in the pixel circuit can be decreased, and the circuit configuration can be simplified.

#### INDUSTRIAL CAPABILITY

[0267] According to the pixel circuit, display device, and method of driving a pixel circuit of the present invention, even when the current-voltage characteristic of a light emitting element changes due to aging, source-follower output without a luminance deterioration can be obtained, the source-follower circuit of the n-channel transistor becomes possible. In addition, it is possible to display uniform and high quality images without regard to variations of the threshold values and mobilities of the active elements inside the pixels. Therefore, the present invention can be applied to electronic devices such as display devices for personal digital assistants, personal computers, and car navigation systems, mobile phones, digital cameras, and video cameras.